Roll No. .....

22148

M. E. 1st Semester
(Electronics & Communication Engg.)
Examination – January, 2012

ELECTRONICS SYSTEM DESIGN

Paper : MEEC-502

Time : Three hours] *[Maximum Marks : 100*

Before answering the questions, candidates should ensure that they have been supplied the correct and complete question paper. No complaint in this regard, will be entertained after examination.

Note : Attempt any *five* questions.

1. (a) Discuss the various operation modes of shift register. 10

(b) What are the various design steps of asynchronous mode. 10

2. (a) Design a circuit to convert D Flip Flop to JK Flip Flop. 10

(b) Why are comparators required ? Design a two bit comparator.

3. (a) Define tristate logic circuit. Further explain how it helps in building tristate bus system. Also state its advantage in reducing hardware in system implementation. 10

(b) State the design steps for next state decodes. 10

4. (a) What is electromagnetic interference in digital circuits & what are the ways we can avoid it. 10

(b) Explain the design steps of asynchronous machines. 10

5. (a) Design a circuit that will compare two 2-bit numbers. Implement the circuit using only NOR gates. 10

(b) Again design the above circuit using only NAND gates. 10

6. (a) Explain briefly the MDS diagram construction concepts with flow diagram.

(b) Describe in brief how a digital system can be interfaced with fibre cable & coaxial cables. 10

7. (a) Convert 632.7184 into binary, octal and hexadecimal. 6

(b) Perform the subtraction on the following numbers using 9's and 10's complement. 6

(i) 540 – 370

(ii) 991 – 762

(c) Implement the following function using 4 × 16 decoder with low asserted outputs : 8

(i) $F_1 (A, B, C, D) = \Sigma (1, 3, 4, 5, 9)$

(ii) $F_2 (A, B, C, D) = \Sigma (1, 4, 5, 6, 7)$

8. Write a short note on any *two* of the following : 20

(a) Races, cycles, hazards,

(b) Design for testability,

(c) FPGA
